SP8620

400MHz ÷ 5

The SP8620 is an asynchronous emitter coupled logic counter which provides an ECL compatible output when an external pulldown resistor is added. It requires an AC coupled input of 600mV p-p.

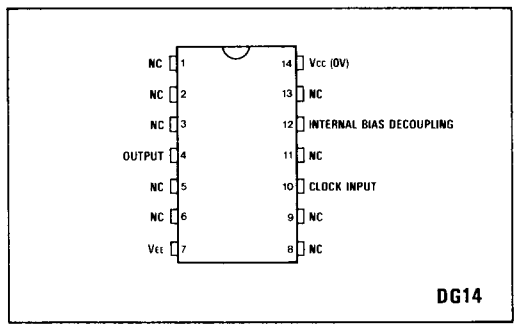


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 285mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	15mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8620 A DG
SP8620 B DG
SP8620 AB DG
SP8620 AC DG

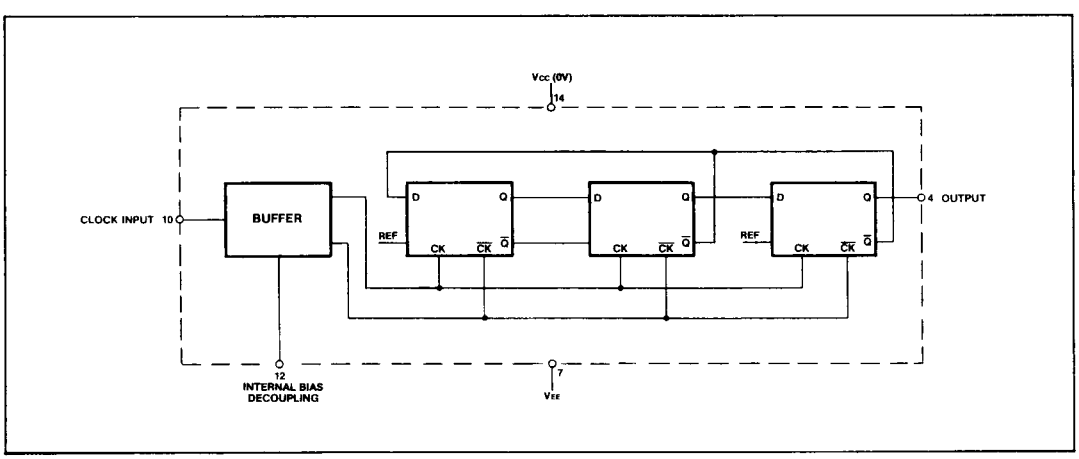


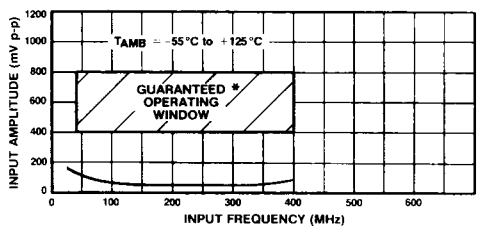
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Conditions	Note
Maximum frequency (sinewave input)	f_{max}	400		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		55	mA	V_{EE} = -5.2V	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8620A

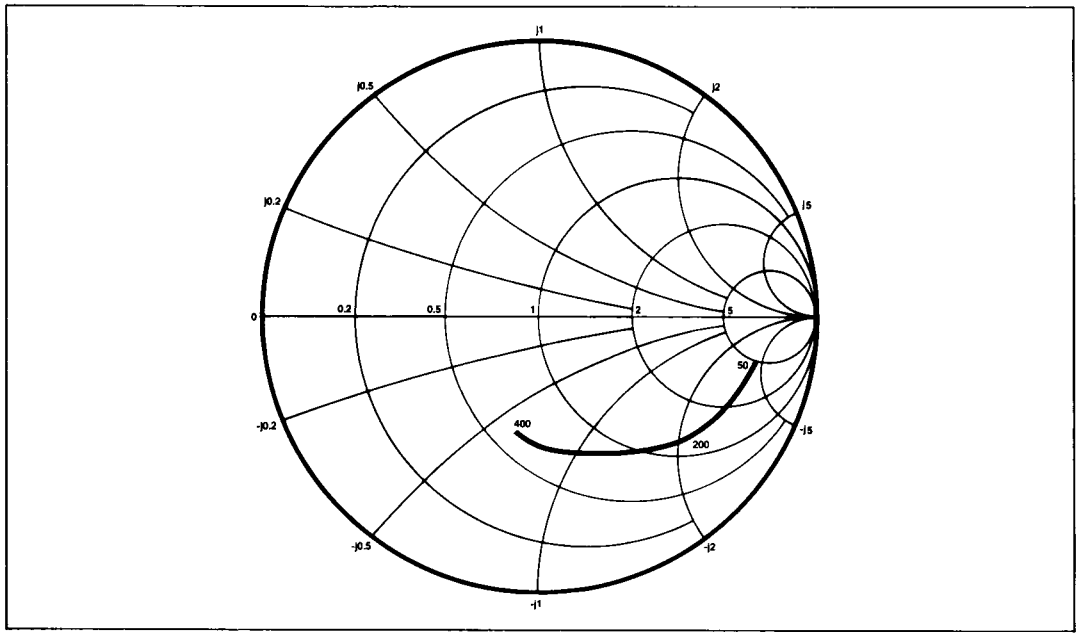


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. The circuit will operate down to DC but slew rate must be better than 100V/μs.
3. The outputs are compatible with ECL II. There is an internal load of 3k at the output. The output can be interfaced to ECL/10K by the addition of 1.5k to the output to increase the output voltage swing.
4. Input impedance is a function of frequency. See Fig.4.
5. All components should be suitable for the frequency in use.

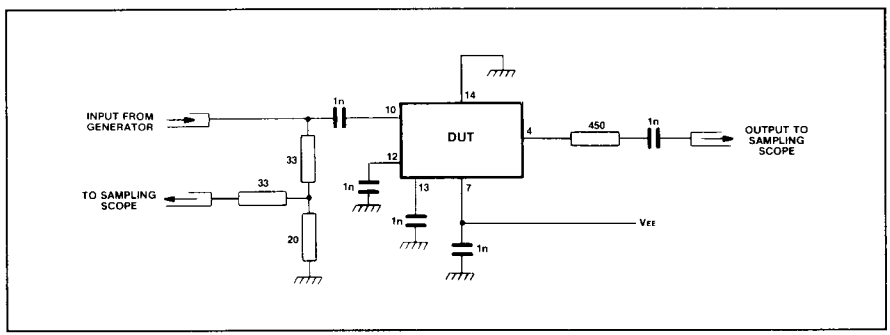


Fig.5 Test circuit

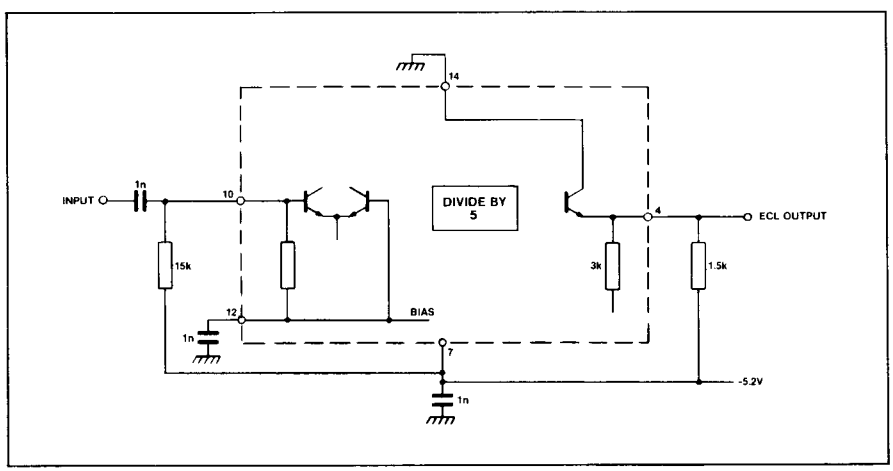


Fig.6 Typical application showing interfacing